## CMOS integration of the suspended gate FET gas sensor

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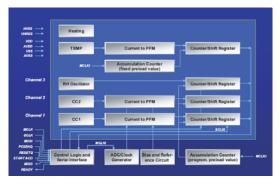
Field effect transistor based chemical and gas sensing began in the early 70s. It was Bergfeld who introduced the ISFET, a FET where the gate metallization was left away. Originally indented for biomedical applications, the ISFET proved to be a tool to measure concentration changes of a particular ion species in liquids. At the same time the application as a gas sensor was studied. While Lundström introduced the Pd gated FET for H2 measurements, Janata exposed the gate via a gap. This construction is now commonly referred to, as the SGFET. Several variants of gate assembly, fabrication and materials were introduced and evaluated, but the read out device was still an ISFET.

The problems in ISFET fabrication and the geometrical coupling of ISFET and suspended gate were overcome by the introduction of the CCFET. Further developments of the concept like compensation of the temperature dependence of the read out devices and approaches to limit the parasitic surface conductivity were introduced.

The attractive potential of the CCFET derives from its capabilities as a platform technology. Only the selection of the respective gate material defines to which gas species the sensor will be sensitive. Considerable efforts were spent, to evaluate different layer materials. Several layers were introduced for different applications:

Gas-Sensitive	Pt	H2
Layer	CuPhC	NO2
Suspended Gate	TiN	NH3
GASE Chip Floating Read-out	GOx	VOC
Electrode Transistor	HPS	CO2

Due to the hybrid integration of CMOS chip and suspended gate, the process options for the layer fabrication are not limited in terms temperature budget and materials. This can be seen as a significant advantage of the CCFET concept.



In a recent announcement Micronas GmbH has presented a fully integrated gas sensing chip, which includes 2 CCFET sensing channels, 1 humidity sensor and a temperature sensor. The further architecture consists of signal conditioning, AD-converter and digital interface (SPI). Via pulsed operation the chip can be operated at extremely low levels of medium power consumption.

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